



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,460	07/30/2003	Darel Emmot	200205912-1	9164

22879 7590 03/30/2007
HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER

DANG, KHANH

ART UNIT	PAPER NUMBER
----------	--------------

2111

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/630,460

Applicant(s)

EMMOT ET AL.

Examiner

Khanh Dang

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 January 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amendments to claims 1, 11, and 20 constitute new matter. If Applicants disagree, Applicants are requested to point to the original filed specification by citing page and line numbers for support.

Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 20, the language "comprises a plurality of signal of signal lines of the system bus" is unclear. Further, it is unclear what may be included in the "collectively, the conductive pins of the integrated circuit component."

Claims 1-10 are directed to an apparatus. However, the essential structural cooperative relationships between elements in the claims such as "logic" (line 2), "logic" (line 4), "logic for controlling," "first portion of system bus," "second portion of system bus," "integrated circuit component," and "second integrated circuit component"

have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

Claims 10-19 are directed to an apparatus. However, the essential structural cooperative relationships between elements in the claims such as “first logic”, “second logic”, “logic for controlling,” “portion of system bus,” “plurality of companion integrated circuit components” “integrated circuit component,” and “remote component” have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

Claims 20-24 are directed to an apparatus. However, the essential structural cooperative relationships between elements in the claims such as “first set of conductive pins,” “second of conductive pins,” “additional conductive pins,” “portion of a system bus,” “integrated circuit component,” and “companion integrated circuit component” have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

MPEP 2172.01 requires that relationships between elements recited in claims must be specified. Specifically, MPEP requires interrelation and structural relationships between essential elements in the claims. It is the Examiner’s position that, the claimed elements, as defined in the originally filed specification and identified above, are essential elements to the claimed invention. Since they are essential elements as defined by the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also the Examiner’s position that the claimed elements as identified above, function simultaneously, are directly

functionally related, directly intercooperate, and/or serve independent purposes, as evidenced from the originally filed specification. If Applicants do not agree with the Examiner that the claimed elements as defined by the specification and identified above, are not essential elements to the claimed invention, Applicants are required to state on the record that this is the case.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

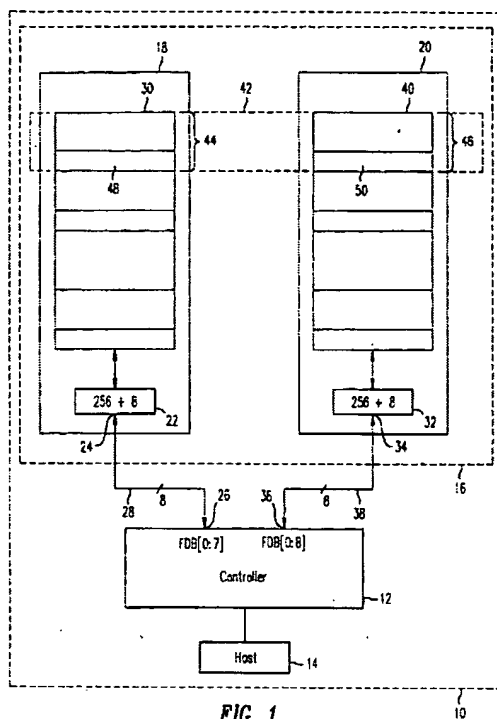
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

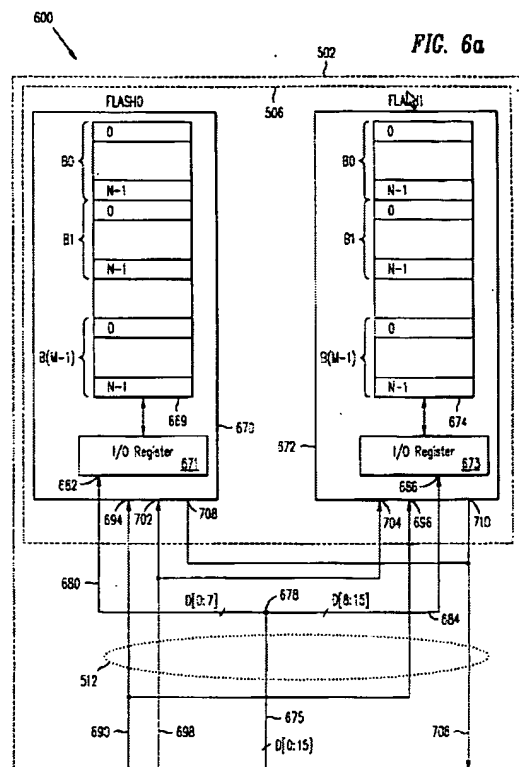
Claims 1, 2, 4-13, and 15-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Estakhri et al. (Estakhri, 6,172,906).

At the outset, it is noted that new limitations added to the claims by the amendment filed 2/2/2007 will be fully addressed under “Response to Arguments.”

As broadly drafted, these claims do not define any structure that differs from Estakhri.

With regard to claim 1, Estakhri discloses an integrated circuit component (Figs. 1 and 6a, shown below:)





comprising: logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises “logic”; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a first portion of a system bus (28/680; column 1, line 31 to column 2, line 3; column 7, line 1-9); and logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called “logic”; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a companion integrated circuit (18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) and to receive information

that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684; column 1, line 31 to column 3, line 2; column 7, lines 1-9).

With regard to claim 2, Estakhri further discloses a link layer control logic in both the logic capable of being configured to interface with the first portion of the system bus and the logic capable of being configured to interface with the companion integrated circuit (it is clear that the controller (12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) linking both logics to provide unified bus logic configured to consolidate information received from both logics interfaced with the first portion of the system bus (28/260; column 1, line 31 to column 2, line 3; column 7, line 1-9) and the companion integrated circuit 18/670 or 20/672), the link layer control logic (12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) being configured to exchange link layer control information, such that both the logic capable of being configured to interface with the first portion of the system bus and the logic capable of being configured to interface with the companion integrated circuit (both logics interfaced with the first portion of the system bus (28/680; column 1, line 31 to column 2, line 3; column 7, line 1-9) and the companion integrated circuit 18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) possess complete link layer control information for the data being communicated over the system bus (it is clear that the controller (12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) provides unified bus logic configured to consolidate information received from both logics interfaced with the first portion of the system bus (28/680; column 1, line 31 to

Art Unit: 2111

column 2, line 3; column 7, line 1-9) and the companion integrated circuit 18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65).

With regard to claim 4, it is clear that the controller (12/510) provides unified bus logic configured to consolidate information received from both logics interfaced with the first portion of the system bus 28/260 and the companion integrated circuit 18/670 or 20/672).

With regard to claim 5, it is clear that the controller (12/510) or the so-called "functional logic" performs at least one logic operation for the integrated circuit component.

With regard to claim 6, it is clear that the system bus comprising two split buses 28/260 and 38/684 is a point-to-point serial communication bus.

With regard to claim 7, it is clear that the memory controller (12/510) or the so-called "functional logic" performs the logic operation of a memory controller.

With regard to claim 8, it is clear that the memory controller (12/510) comprises logic capable of configuring the integrated circuit component (18/670) for operation with a companion integrated circuit component (20/672).

With regard to claim 9, it is clear that memory controller (12/510) comprises logic capable of configuring either the integrated circuit component (18/670) or (20/672) for operation in a stand-alone configuration.

With regard to claim 10, it is clear that the first portion of the system bus is substantially one-half of the system bus and the second portion of the system bus is a remainder of the system bus (see at least column 7, lines 4-9).

With regard to claim 11, Estakhri discloses a system comprising: a plurality of companion integrated circuit components (18/670, 20/672) that collectively implement a logic function embodied in a single, conventional integrated circuit component (shown generally at Fig. 1, 6(a, b), each companion integrated circuit component (one of 18/670, 20/672) comprising: a first logic interface for communicating with a remote component via a portion of a system bus (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "first logic interface" for communicating with a remote component via a portion of a system bus 28/260); a second logic interface for communication with companion logic interfaces of the remaining of the plurality of the integrated circuit components over a separate bus (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "second logic interface" capable of being configured to interface with a companion logic interfaces of the remaining of the plurality of integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684); and logic (memory controller (12/510) for controlling the selective communication of information received from the first logic interface (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "first logic interface" for

Art Unit: 2111

communicating with a remote component via a portion of a system bus 28/260) via the portion of the system bus through the second logic interface to the companion integrated circuit (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "second logic interface" capable of being configured to interface with a companion logic interfaces of the remaining of the plurality of integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684).

With regard to claim 12, as discussed in claim 11, the logic for controlling the selective communication of information received from the first logic interface through the second logic interface further includes first split bus logic configured to interface with the first logic interface, and second split bus logic configured to interface with the second logic interface (the system bus of Estakhri comprises a first split bus and a second split bus ;see at least column 7, lines 4-9).

With regard to claim 13, the link layer control logic in both first split bus logic and the second split bus logic (it is clear that the controller (12/510) provides unified bus logic configured to consolidate information received from both bus logics), the link layer control logic being configured to exchange link layer control information, such that both the first split bus logic and the second split bus logic possess complete link layer control information for the data being communicated over the system bus (it is clear that the

Art Unit: 2111

controller (12/510) provides unified bus logic configured to consolidate information received from both bus logics).

With regard to claims 15-19, see discussion above, since the subject matter presented in claims 15-19 has already been addressed above).

With regard to claim 20, Estakhri discloses an integrated circuit component comprising: a first set of conductive pins for channeling communications with a remote component via a portion of a system bus (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "first logic interface" for communicating with a remote component via a portion of a system bus 28/260; note also that it is inherent that pins must be provided for connections between discrete chips or ICs); a second set of conductive pins for channeling communications with a companion integrated circuit component (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "second logic interface" capable of being configured to interface with a companion logic interfaces of the remaining of the plurality of integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684); note also that it is inherent that pins must be provided for connections between discrete chips or ICs); additional conductive pins for carrying additional control and communication signals (it is clear that additional pins in addition to the conductive

Art Unit: 2111

pins discussed above must be used in the IC of Estakhri); wherein the number of total conductive pins of the integrated circuit component is fewer than the number of conductive pins of a corresponding conventional integrated circuit component (as best the examiner can ascertain, the number of total conductive pins of the integrated circuit component of Estakhri is fewer than the number of conductive pins of a corresponding conventional integrated circuit component, since split bus system is used for each IC component).

With regard to claims 21-23, see discussion above, since the subject matter presented in claims 21-23 has already been addressed above.

With regard to claim 24, it is clear that "conductive pins" must also be provided so that different ICS (as identified above) can be connected to one another.

Response to Arguments

Applicants' arguments filed 1/3/2007 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris*, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997). As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification

Art Unit: 2111

cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112 Rejection:

With regard to the rejection of claims 1-24 in view of MPEP 2172.01, Applicants argue that "Applicants respectfully request the Examiner to provide more helpful insight into this rejection (either by more fully stating the rejection or by providing exemplary language that would overcome the rejection), should the Examiner disagree with Applicants' position and maintain this rejection. In reconsidering this rejection, however, Applicants remind the Examiner that claim breadth should not be confused with indefiniteness (see MPEP 2173.04)."

At the outset, it is noted that Applicants' same request for assistance has already been responded by the Examiner in the previous Office Action. In any event, in response to Applicants' request for assistance, once again, the word(s): -- connected— or --operatively connected -- may be used to provide essential structural cooperative relationships between structural elements recited in the claims.

The 102 Rejection:

With regard to claim 1, Applicants argue that "claim 1 is directed to "an integrated circuit component" (i.e., a single component) that includes two separate logic blocks. A first logic block is capable of being configured to interface with a first portion of a system bus. Likewise, the second logic block is capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus. Simply stated, these features are not disclosed in the '906 patent."

Contrary to Applicants' argument, Estakhri discloses an integrated circuit component (Figs. 1 and 6a) comprising: logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises "logic"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a first portion of a system bus (28/680; column 1, line 31 to column 2, line 3; column 7, line 1-9); and logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "logic"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a companion integrated circuit (18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) and to receive information

that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684; column 1, line 31 to column 3, line 2; column 7, lines 1-9). Further, it is clear from at least Fig. 6a of Estakhri that the first companion integrated circuit (18/670) and the second companion integrated circuit (20/672) each is disposed in a single integrated circuit chip.

Applicants also argue that "[t]he teachings applied by the Office Action from the '906 patent (disclosing two memory chips 670 and 672 of a memory bank 506) are simply inapplicable to the embodiments defined by claim 1. In this regard, the two memory chips 670 and 672 of the '906 patent are separate integrated circuits, and not a single integrated circuit as required by claim 1."

Contrary to Applicants' argument, it is clear from at least Fig. 6a of Estakhri that the first companion integrated circuit (18/670) and the second companion integrated circuit (20/672) each is disposed in a single integrated circuit chip.

Applicants also argued that:

The FINAL Office Action responded to this previous argument by citing FIGs. 1 and 6. It appears that the Examiner is treating the reference number 600 (of the '906 patent) in FIG. 6, for example, as denoting a chip. However, it instead denotes an entire memory system. The specification of the '906 patent confirms this (see col. 6, line 36 and col. 7, lines 47-52). Indeed, the FINAL Office Action (p. 15) states:

Contrary to Applicants' argument, it is clear from at least Fig. 6a of Estakhri that the first companion integrated circuit (18/670) and the second companion integrated circuit (20/672) each is disposed in a single integrated circuit chip.

This position reflects at least one fundamental misapplication of Estakhri to claim 1. As set forth above, reference number 600 (of Fig. 6a) denotes a "memory system" (col. 6, line 36), and not a single integrated circuit. Reference number 506 denotes a "memory bank" (col. 6, line 57), and not a single integrated circuit. Finally, by the Examiner's own admission that reference number 670 comprises a first integrated circuit and reference number 672 comprises a second integrated circuit, the two separate integrated circuits cannot properly/logically comprise a single integrated circuit chip, as expressly claimed by claim 1.

Contrary to Applicants' argument, it is clear that the memory system or flash memory system of Estakhri is a memory chip. See definition of Flash Memory by Techencyclopedia, cited below.

Further, in anticipation that Applicants will address the issue of new matter, regarding the new limitations added to the claims, it is clear that each bus

portion of the system bus of the '906 patent comprises a plurality of separate and different signal lines. See at least column 7, lines 1-9.

With regard to claim 11, Applicants argue that "the Office Action cites memory chips 670 and 672 as comprising the claimed "integrated circuit." It then cites register 671 as comprising the claimed first logic interface. Then, the Office Action cites the same register 671 as comprising the claimed second logic interface. This rejection simply makes no sense, in the context of the claimed embodiments. In this regard, the first logic interface is specifically claimed as "communicating with a remote component via a portion of a system bus." In contrast, the second logic interface is specifically claimed as being configured for "communication with companion logic interfaces of the remaining of the plurality of the integrated circuit components over a separate bus." This is not taught or disclosed in the '906 patent. In fact, the only input to the applied I/O register 671 is bit positions D[0:7] of the data bus 680. These bit positions couple to I/O register 671 at reference number 682. Significantly, the register 671 cannot comprise the claimed second logic interface, assuming that that register 671 comprises the first logic interface. Furthermore, the I/O registers 671 and 673 are disposed in separate integrated circuit chips, so these elements cannot be mixed and matched as applying to the first and second logic interfaces, as claim 11 requires that the first and second logic interfaces be in a single integrated circuit component.

Contrary to Applicants' argument, Applicants are claiming different logic interfaces, namely "first logic interface" and "second logic interface", provided by an IC component. Applicants are NOT claiming two different and separate structural devices

or circuits residing inside an IC component. It is clear that any conventional IC component can provide different logics, not necessarily implemented by hardware, but also by software, to enable the IC component to communication with other ICs or circuitries. In the instant case, it is clear that the I/O register provides logics for the memory chip 670, for example, to enable the memory chip to communicate with the bus or with another memory chip (672, for example). By definition, reading an I/O register involves accessing to its memory.

With regard to claim 20, Applicants argue that "the Office Action further concluded that "it is inherent that pins must be provided for connections between discrete chips or ICs." Finally, the Office Action alleged that "the number of total conductive pins of the integrated circuit component of Estakhri is fewer than the number of conductive pins of a corresponding conventional integrated circuit component, since split bus system is used for each IC component." In essence, the rejection of claim 20 appears to take the position that the recited features are inherent in the structure recited in claims 1 or 11, and then relies on the rejections of those claims. In response, Applicants repeat and reallege the responsive remarks (above) with respect to the inapplicability of the '906 patent to claims 1 and 11."

In response to Applicants' argument, see discussion above, since Applicants state that "Applicants repeat and reallege the responsive remarks (above) with respect to the inapplicability of the '906 patent to claims 1 and 11."

Thus, as best the Examiner can ascertain from the language of claim 20, the Examiner maintains his position that Estakhri discloses an integrated circuit component

comprising: a first set of conductive pins for channeling communications with a remote component via a portion of a system bus (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "first logic interface" for communicating with a remote component via a portion of a system bus 28/260; note also that it is inherent that pins must be provided for connections between discrete chips or ICs); a second set of conductive pins for channeling communications with a companion integrated circuit component (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "second logic interface" capable of being configured to interface with a companion logic interfaces of the remaining of the plurality of integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684); note also that it is inherent that pins must be provided for connections between discrete chips or ICs); additional conductive pins for carrying additional control and communication signals (it is clear that additional pins in addition to the conductive pins discussed above must be used in the IC of Estakhri); wherein the number of total conductive pins of the integrated circuit component is fewer than the number of conductive pins of a corresponding conventional integrated circuit component (the number of total conductive pins of the integrated circuit component of Estakhri is fewer than the number of conductive pins of a corresponding conventional integrated circuit

component, since split bus system is used for each IC component. As conductive pins must be provided for signal lines of a system bus, a portion of the system bus would require less signal lines and thus, fewer conductive pins).

US Patent Nos. 7099994 and 7103826 are cited as relevant art. Applicants are reminded of Applicants' "Duty of Disclosure, Candor, and Good Faith." See MPEP 2001 and 37 CFR 1.56 (a). Throughout prosecution of this application and of another pending application (now on appeal) before this Examiner, Applicants, in both applications, fail to provide this Office with all information known to be material to each application. Specifically, Applicants have filed multiple related applications without providing any information to this Office that these applications are closely related. Applicants are also reminded that "no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct."

Allowable Subject Matter

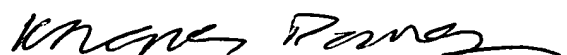
Claims 3 and 14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**Khanh Dang
Primary Examiner**